Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently Amended) A semiconductor component with trench isolation for defining active regions in a semiconductor substrate, the trench isolation comprising:

a deep isolation trench with a first covering insulation layer below a surface of the semiconductor substrate and a second covering insulation layer over the first covering insulation layer and above the surface of the semiconductor substrate, a gate oxide layer over a surface of the second covering insulation layer, a side wall insulation layer, an electrically conductive filling layer, which is electrically connected to a predetermined doping region of the semiconductor substrate in a bottom region of the isolation trench, and wherein the first covering insulation layer is over a top surface of the electrically conductive filling layer, and the sidewall insulation layer; and further comprising:

a trench contact, which comprises:

a deep contact trench with a side wall insulation layer and an electrically conductive filling layer which is electrically, contact-connected to the predetermined doping region of the semiconductor substrate in a bottom region of the contact trench;

a trench contact insulation layer being only above a surface of the electrically conductive filling layer; and

a contact opening through the trench contact insulation layer and in contact with a top surface of the electrically conductive filling layer, and

wherein a composition of the electrically conductive filling layer that is electrically, contact-connected to the predetermined doping region of the semiconductor substrate

in a bottom region of the contact trench is the same as a composition of the electrically conductive filling layer having a top surface in contact with the contact opening.

2. (Previously Presented) The semiconductor component of claim 1, wherein the first covering insulation layer is within the isolation trench.

3. (Previously Presented) The semiconductor component of claim 1, wherein the trench isolation and the trench contact have a larger depth than an associated depletion zone in the semiconductor substrate.

4. (Previously Presented) The semiconductor component of claim 1, wherein the trench isolation further comprises a widened, shallow isolation trench at a surface of the semiconductor substrate configured for filling non-active regions.

5. (Previously Presented) The semiconductor component of claim 1, wherein the predetermined doping region comprises a doping well comprising a multiple well structure.

6. (Previously Presented) The semiconductor component of claim 1, wherein the semiconductor substrate comprises Si, the second covering insulation layer and side wall insulation layer comprise SiO2, and the electrically conductive filling layer comprises highly doped polysilicon.